REMARKS

The Office Action of December 29, 2011, was received and carefully reviewed. Claims 1-19 and 33-35 were pending in this application prior to the instant amendment. By this amendment, claims 1-8 and 33 are amended. No new matter has been added. Thus, claims 1-19 and 33-35 remain currently pending for consideration.

Claim Rejections Under 35 U.S.C. §§ 102 and 103

Claims 1-10, 16, 18, 19 and 33-35 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. App. Pub. No. 2002/0030189 A1 to Ishikawa et al. ("Ishikawa"), or, in the alternative, as obvious over Ishikawa, in view of U.S. Patent No. 6,211,067 B1 to Chen ("Chen"). Claims 11 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishikawa, in view of U.S. Pat. App. Pub. No. 2002/0132396 A1 to Yamazaki et al. ("Yamazaki"). Claims 13 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishikawa. Claims 14 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishikawa, in view of U.S. Pat. App. Pub. No. 2001/0013913 A1 to Young ("Young"). These rejections are traversed at least for the reasons advanced in detail below.

I. Independent Claims 1-8

In the Office Action, the Examiner asserts that FIG. 15B of Ishikawa shows a second conductive layer on and in contact with a first insulating layer 402 and a first conductive layer, by relating the claimed first and second conductive layers to the impurity regions of Ishikawa. *See, page 6 of the Office Action*. Without conceding in detail the merits of the Examiner's rejection, Applicants herein amend independent claims 1-8 to recite, *inter alia*, "a second conductive layer including at least one of Ag, Au, Pt, Ir, Rh, W, Al, Cd, Zn, Zr, Ba, In on and in contact with the first insulating layer and the first conductive layer" (*emphasis added*). Support for this amendment can be found, for example, in paragraph [0017] of the instant application's publication, U.S. Pat. App. Pub. No. 2007/0085938 A1 ("the '938 publication"). Applicants note that Ishikawa is entirely silent as to the inclusion of these newly recited elements in any of the disclosed impurity regions 406, 410, 412, 2407, 2411 or 2413. *See, for example, paragraph [0292] and [0298] of Ishikawa.*

II. Independent Claims 3-8

With respect to claims 3-8, the Examiner asserts that FIG. 15B of Ishikawa discloses a semiconductor layer over an impurity region with a gate insulating film therebetween, by comparing the claimed semiconductor layer to the gate wiring 409 of Ishikawa. *Id.* Applicants respectfully disagree with this assertion by the Examiner, and note that the gate wiring 409 of Ishikawa comprises a tungsten nitride film and tantalum film, or uses Ta, Ti, Mo, W, Cr, Si, or an alloy film of these elements. *See, paragraphs [0295]-[0296] of Ishikawa*. Thus, gate wiring 409 cannot be considered as "a semiconductor layer", as recited in independent claims 3-8.

III. Independent Claims 5 and 6

With respect to claims 5 and 6, the Examiner asserts that FIGS. 16, 24A and 24B of Ishikawa teach a first electrode 1203 over one of the pair of third conductive layers, an electroluminescent layer 1201 over the first electrode 1203, and a second electrode 1200 over the electroluminescent layer 1201. *See, page 10 of the Office Action*. With respect to claims 7 and 8, the Examiner also asserts that FIG. 16, 24A and 24B of Ishikawa teach a first electrode 1203 over one of the pair of third conductive layers, and a second insulating layer having a second opening over the other one of the pair of third conductive layers. *See, page 16 of the Office Action*. Applicants again respectfully disagree with the Examiner in these regards, and note that FIGS. 24A and 24B fail to show the claimed positional relationships between the components of claims 5-8. Thus, even if FIGS. 24A and 24B were to be combined with FIG. 16, it would fail to arrive at the structure of independent claims 5-8.

IV. Dependent Claims

With respect to dependent claim 9, the Examiner asserts that Ishikawa teaches a thin film transistor or display device further comprising a titanium oxide film below the first conductive layer, and cites adhesive film 420 of FIGS. 14B-C. *See, page 17 of the Office Action*. However, Applicants note that Ishikawa is entirely silent as to a titanium oxide film below the first conductive layer. *See, FIGS. 14B-C and paragraph [0323] of Ishikawa*.

With respect to dependent claim 10, the Examiner asserts that paragraph [0305] of Ishikawa teaches a thin film transistor or display device further comprising a film comprising aluminum. *See, page 18 of the Office Action*. Applicants note, however, that claim 10 further requires that the film be "below the first conductive layer" (*emphasis added*). Further, as shown in FIG. 9B of Ishikawa, source and drain wirings 416 (which the Examiner appears

to relate to the claimed film) are not below impurity regions 412 (which the Examiner compares to the claimed conductive films).

With respect to dependent claim 16, the Examiner asserts FIG. 15B of Ishikawa teaches a thin film transistor, wherein the semiconductor layer is a polycrystalline semiconductor. *See, page 18 of the Office Action*. However, as discussed above with respect to independent claims 3-8, gate wiring 409 of Ishikawa cannot be considered as "a semiconductor layer", as alleged by the Examiner. Nevertheless, Applicants note that Ishikawa fails to disclose that gate wiring 409 "is a polycrystalline semiconductor including at least one of hydrogen and halogen", as claimed.

With respect to dependent claims 14 and 15, the Examiner concedes that Ishikawa fails to teach the use of amorphous or semi-amorphous silicon in the semiconductor layer. *See, page 20 of the Office Action*. Nevertheless, the Examiner asserts that:

> [I]t is widely known in the semiconductor art to use amorphous semiconductor in TFT active areas. For instance, Young discusses in Fig. 4 amorphous semiconductor gate structures. Therefore, the use of amorphous semiconductor material is (*sic*) TFT active regions would have been obvious to one of ordinary skill in the art.

Id. According to the Examiner's interpretation, however, the claimed semiconductor layer corresponds to a gate wiring 409 of Ishikawa. Applicants submit, therefore, that there would be no motivation for one skilled in the art to combine the material of the TFT active layer of Young into a gate wiring, such as gate wiring 409 of Ishikawa.

Conclusion

Thus, Applicants respectfully request the withdrawal of the rejection of independent claims 1-8, and dependent claims 9, 10 and 14-16. The rejection of claims 13, 17-19 and 33-35 is improper at least by virtue of their dependence on one or more of claims 1-8. The rejection of claims 11 and 12 is also improper at least by virtue of their dependence on one or more of claims 1-8, and because Yamazaki fails to overcome the above-noted deficiencies of Ishikawa. The rejection of claims 13 and 17 is improper at least by virtue of their dependence on one or more of claims 1-8, and because Yamazaki fails to overcome the above-noted deficiencies of Ishikawa.

In view of the foregoing, Applicants respectfully request allowance of the instant application. If a conference would be helpful in expediting prosecution of the instant application, the Examiner is invited to telephone the undersigned to arrange such a conference.

Except for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No. 19-2380. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

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